



Explore the Impact of AME on the Bare Die Packaging Industry

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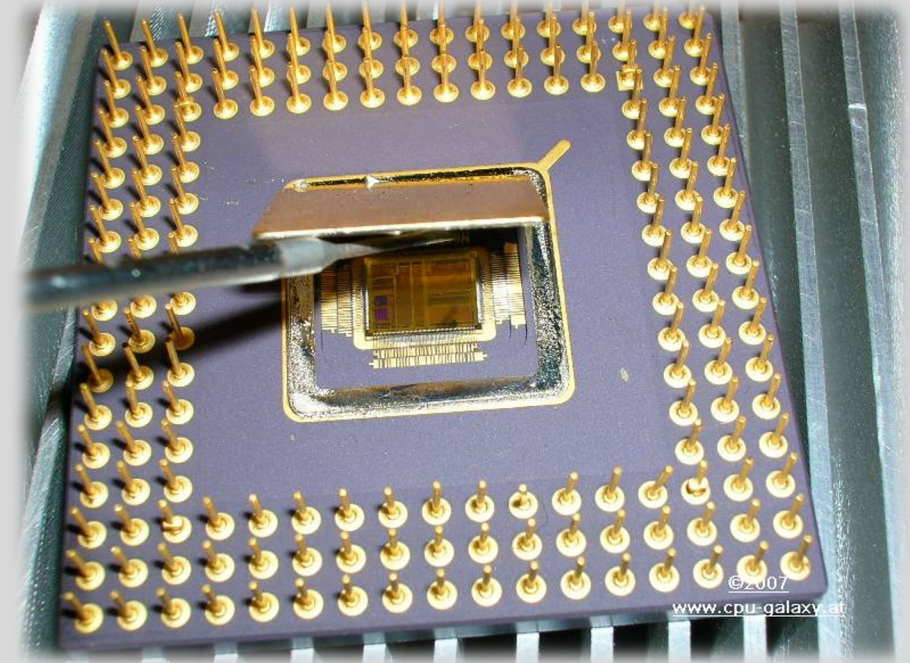
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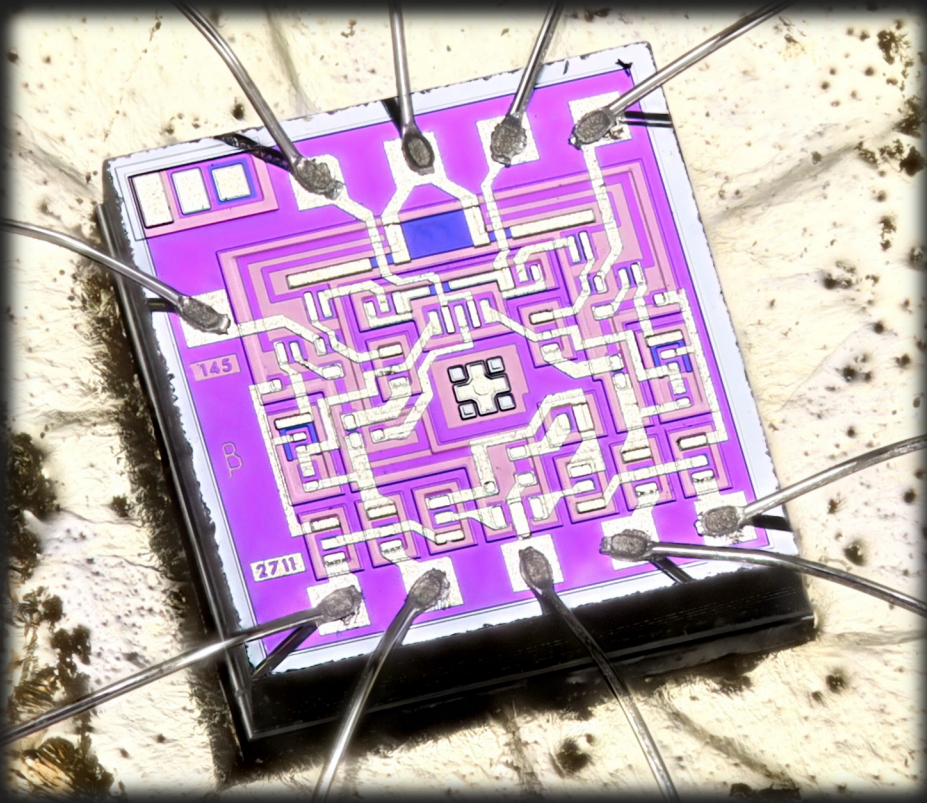
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02 AME Possibilities

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01 Introduction to Semiconductor Packaging





Bare die

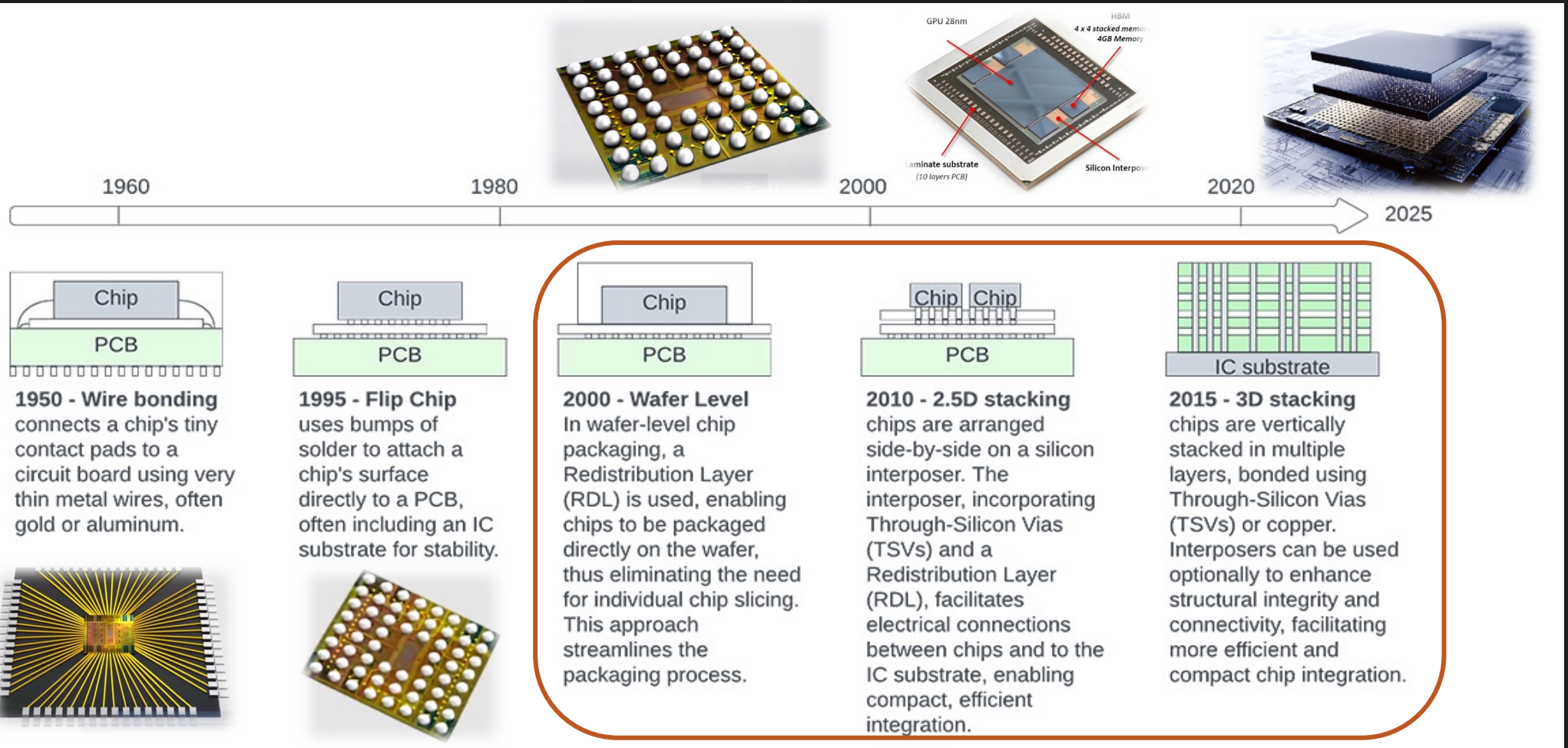
- The heart of a computer
- Small, not encapsulated semiconductor piece, usually made of silicon
- Contains integrated circuits
- In electronics manufacturing, bare dies are directly integrated into devices
- Forms critical building blocks of everyday technology

Why bare dies?

Significance in the electronics industry:

- **Miniaturization of Devices:** Bare dies are crucial for creating smaller, more compact electronic devices.
- **Enhanced Performance:** By eliminating the need for traditional packaging, bare dies facilitate more efficient and direct connections within electronic circuits. This leads to faster data processing and improved overall performance of devices.
- **Cost-Effective Solutions:** Utilizing bare dies can reduce material and manufacturing costs.
- **Customization and Flexibility:** Bare dies offer greater design flexibility, enabling manufacturers to tailor electronic components to specific applications.
- **Improved Heat Dissipation:** Without the constraints of traditional packaging, bare dies can dissipate heat more effectively.
- **Enabling Advanced Technologies:** Bare dies are pivotal in the development of emerging technologies such as Internet of Things (IoT) devices and advanced medical equipment, where space is at a premium and efficiency is paramount.

Historical context



Semiconductor packaging by method

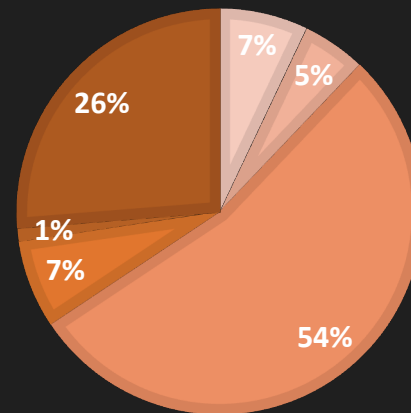
Traditional packaging

Advanced packaging

Wire-Bonding

ESTIMATED MARKET SIZE 2023

■ Fan-in
 ■ Fan-out
 ■ Flip-Chip
■ 3D stacking
 ■ Embedded Die
 ■ Wire bonding



Fan-Out

Fan-In

Flip-Chip

3D stacking

Embedded Die

* Semiconductor packaging market - companies, Share & Trends. Semiconductor Packaging Market - Companies, Share & Trends. (n.d.). <https://www.mordorintelligence.com/industry-reports/semiconductor-packaging-market>

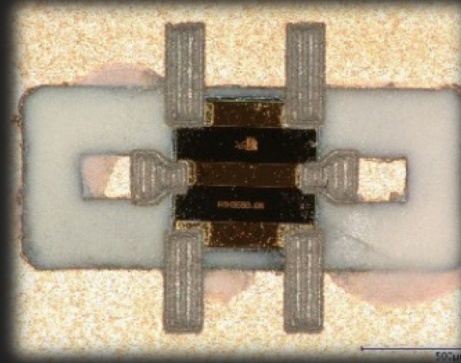
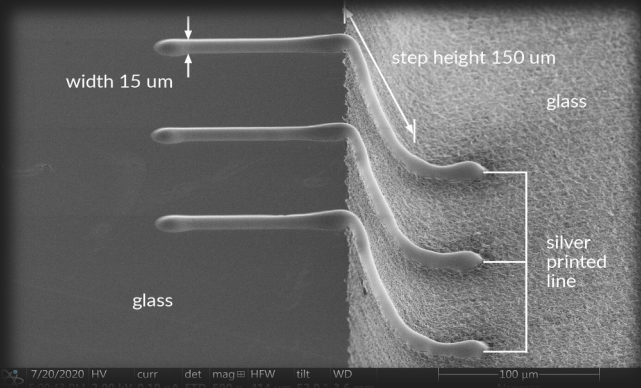
* Semiconductor packaging market (by type: Flip Chip, embedded die, fan-in wafer level packaging, fan-out wafer level packaging; by packaging material: Organic substrate, leadframe, bonding wire, ceramic package, die attach material; by technology: Grid array, small outline package, flat- no lead package, dual in- line package, ceramic dual in- line package; by end-user) - global industry analysis, size, share, growth, trends, regional outlook, and forecast 2023-2032. Precedence Research. (n.d.). <https://www.precedenceresearch.com/semiconductor-packaging-market>

* Precedence Research. (2023, November 23). Semiconductor packaging market size to surpass USD 65.46 billion by 2032. GlobeNewswire News Room. <https://www.globenewswire.com/en/news-release/2023/11/23/2785316/0/en/Semiconductor-Packaging-Market-Size-to-Surpass-USD-65-46-Billion-By-2032.html>

02 AME Possibilities

Semiconductor Packaging limitations and solutions based on AME :

- **Complex Geometries and Miniaturization** – complex production methods struggle to withstand the design complexity.
- **Rapid Prototyping and Design Flexibility** – long preparation time for manufacturing.
- **Materials and Sustainability** – limited and expensive materials.
- **Customization for Specific Applications** – complex preparation equipment.
- **Thermal Management**
- **Integrated Functionality**

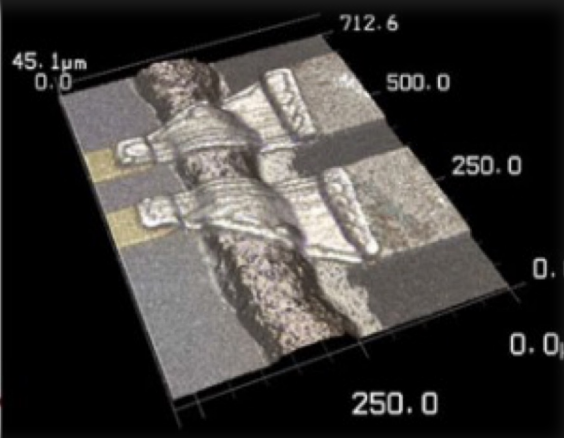
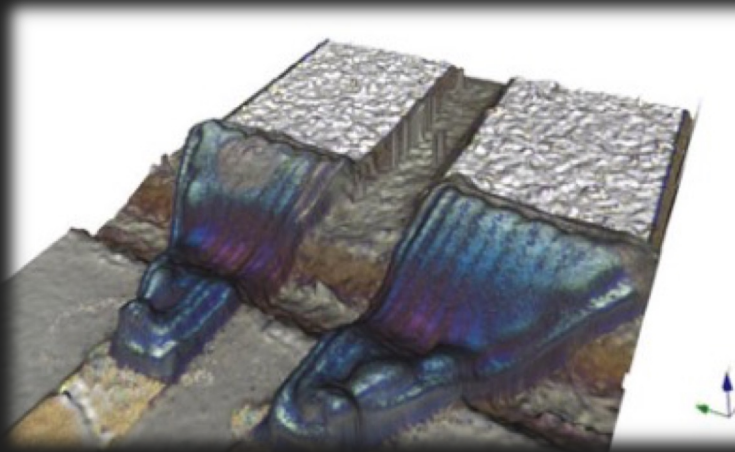


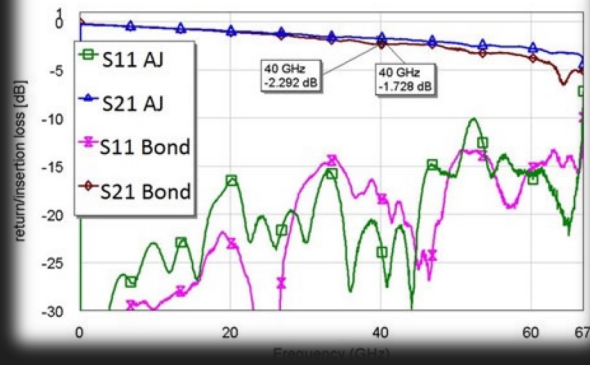
Performance:

- Flexible connection structure
- Flexible dimensions
- Flexible process
- Can create the whole design and not only packaging
- Big material/processes portfolio
- Rapid prototyping

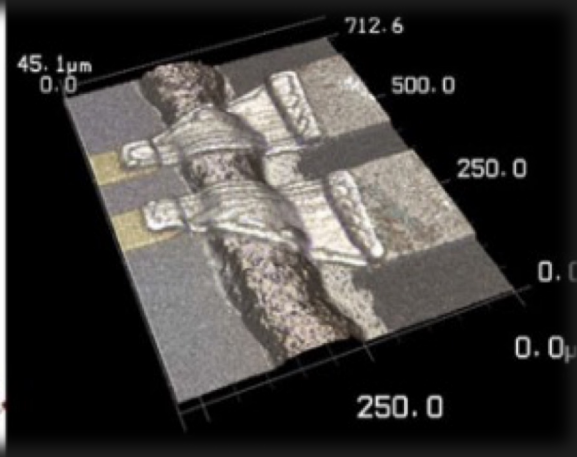
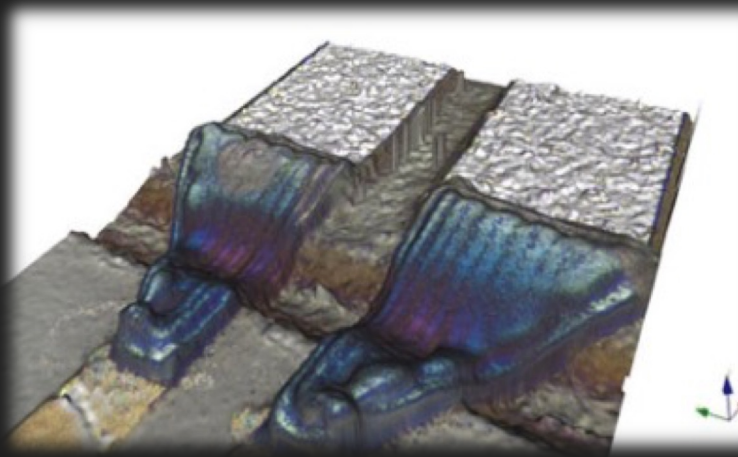
Logistics:

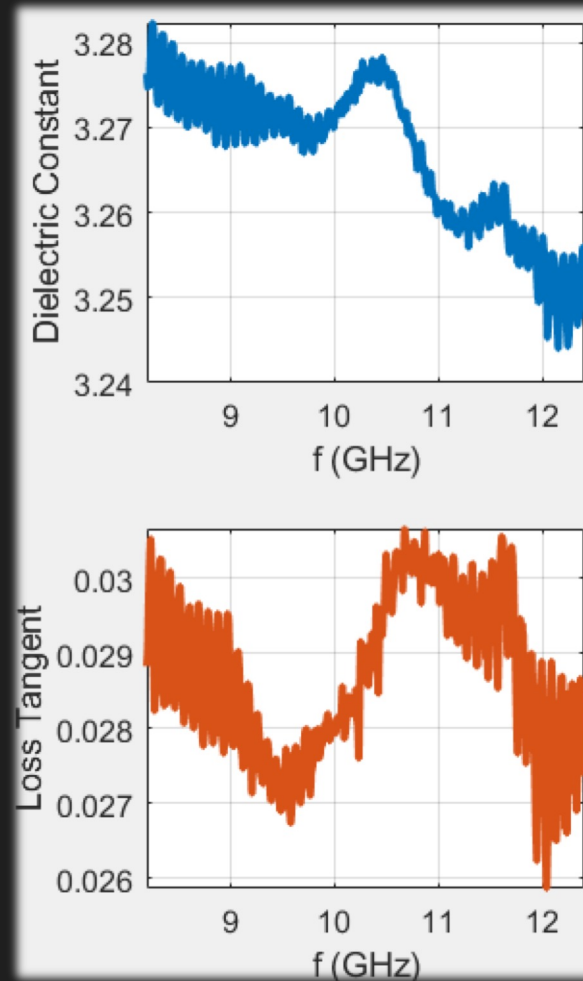
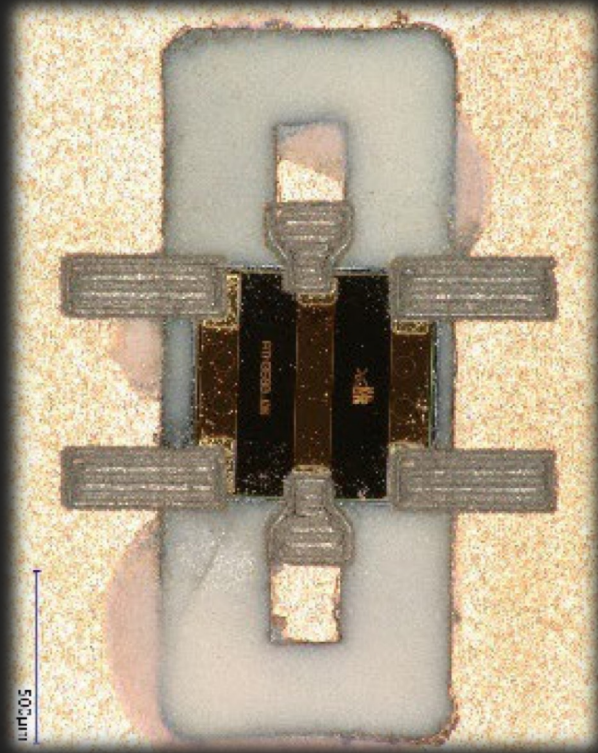
- Versatile solution
- No dedicated calibration is required



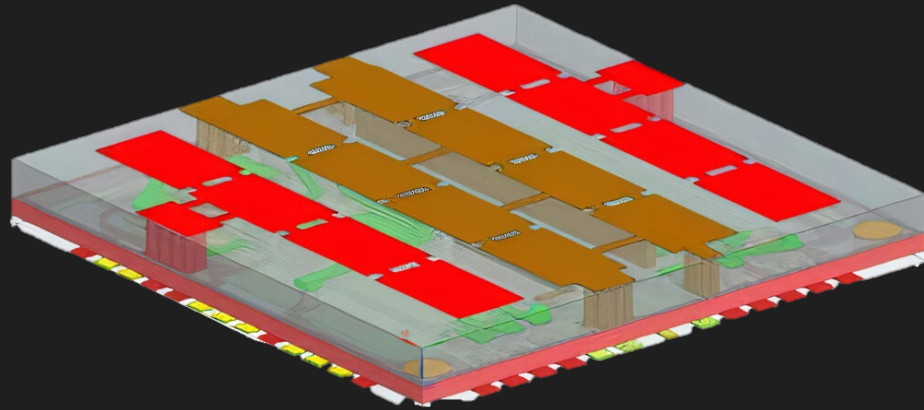


1. **Material Compatibility:** Handles different thermal expansion coefficients.
2. **Reduced Insertion Loss:** Significantly improves signal integrity.
3. **Customizable Impedance:** Enables low-loss, low-reflection connections.
4. **High-Frequency Performance:** Suitable for up to three-digit GHz range.

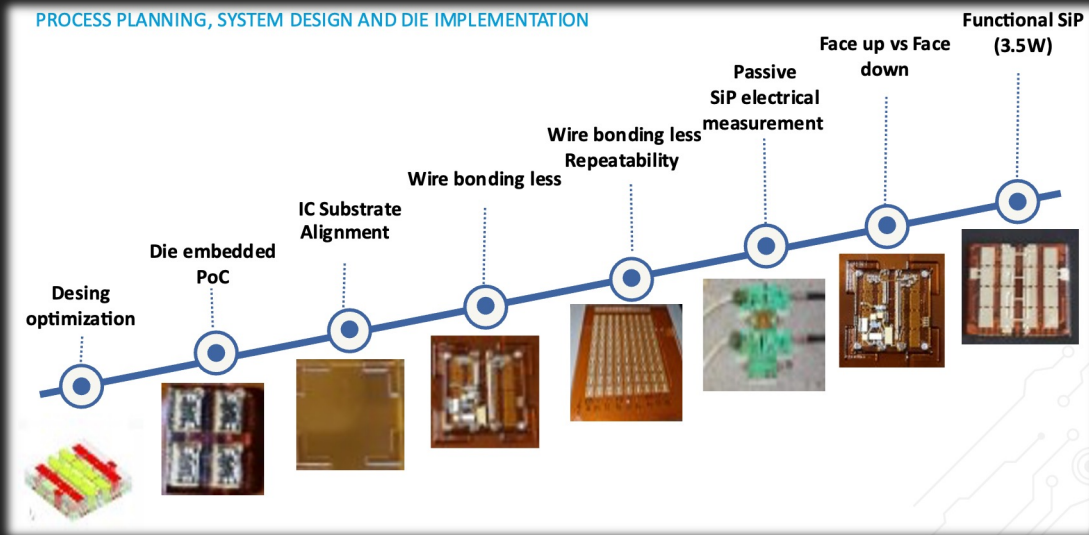




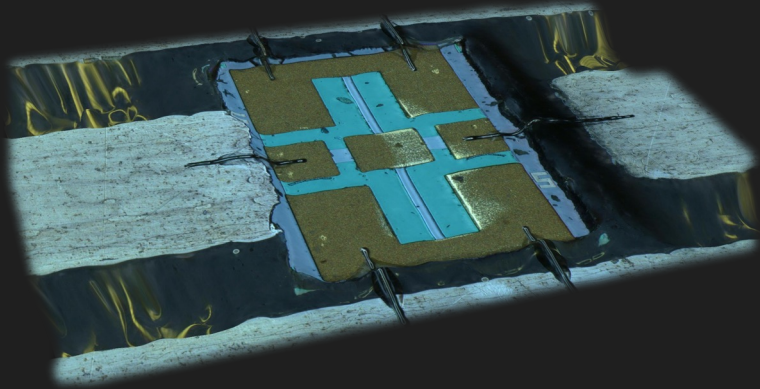
1. **Multi-functionality Integration:** Allows integration of multiple functions in a small space with high resolution.
2. **3D Topology Flexibility:** Enables conformal assembly on 3D geometries, beyond the demonstrated 2D planar topology.
3. **Rapid and Easy Assembly:** Offers faster and simpler assembly compared to conventional methods.
4. **Advantageous for 5G/IoT:** Ideal for creating smart devices with flexible, complex shapes requiring internet connectivity.
5. **Crucial for Wireless Communication Evolution:** Key to advancing 5G/IoT and future high-frequency wireless applications.



1. **Efficient R&D Cycle:** Reduces R&D time from the traditional 12 months to just 2 months.
2. **Prototype Speed:** Allows for rapid prototyping and iteration of new electronic products.
3. **Complex Multilayer Design:** Facilitates the creation of complex, multi-layered SiP designs.
4. **High Precision:** Produces detailed connectors and cavities with high accuracy, eliminating the need for drilling.



03 Showcase of J.A.M.E.S Applications

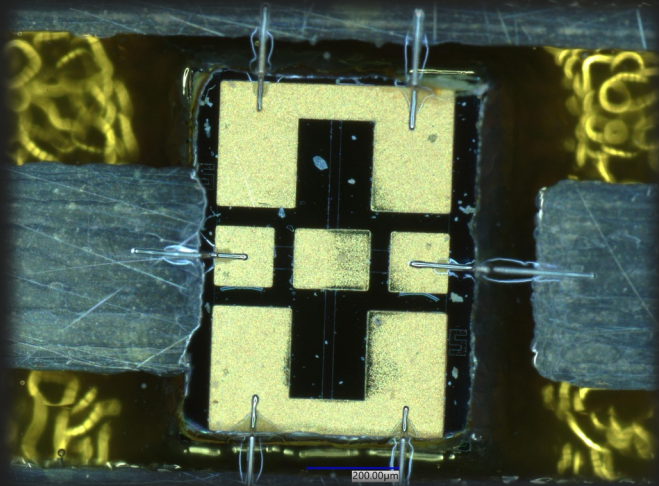


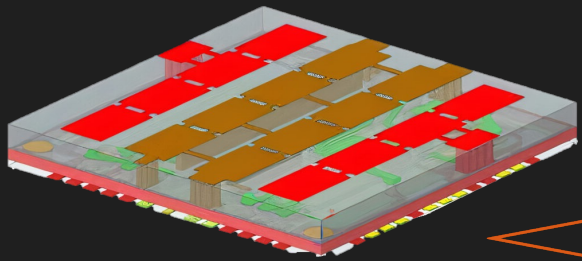
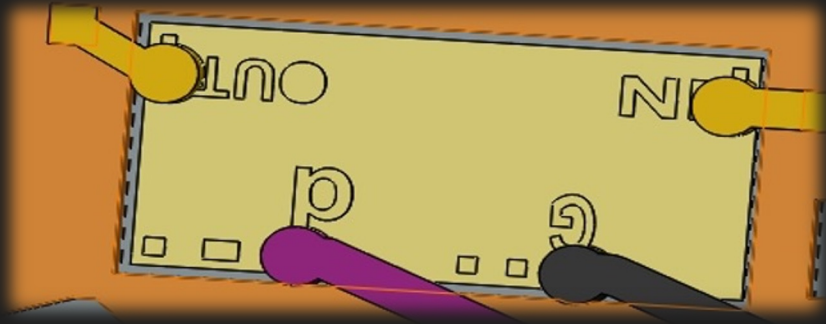
J.A.M.E.S and XTPL collaboration project

RF performance capabilities examination

Key Features:

- Performance.
- Material adhesion
- Combine technologies
- Reduced bonding features
- The way for proper AM packaging process

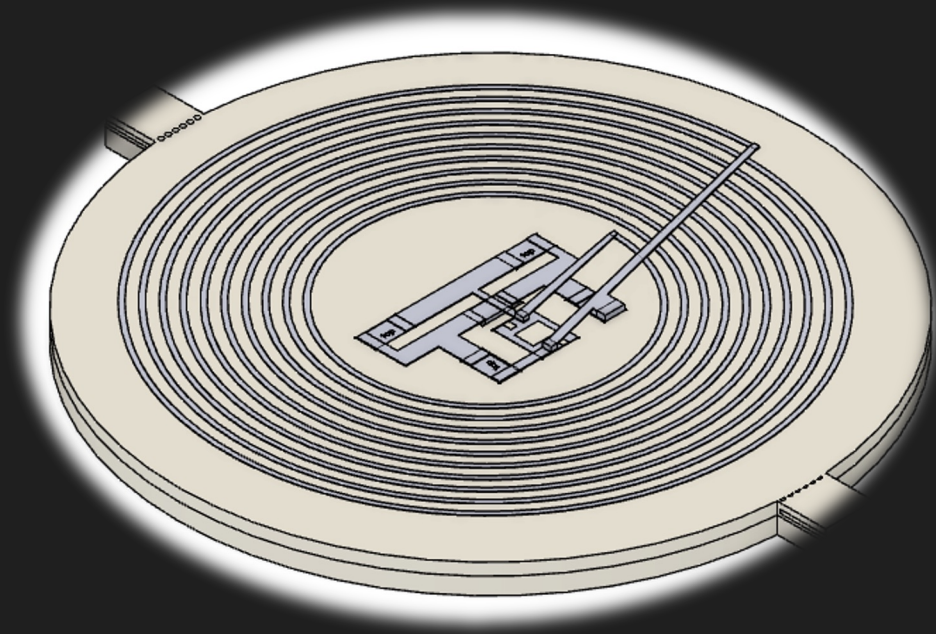




Nano Dimension QuikSiP

Key features

- Avoid chip packages
- Achieve a high level of miniaturization
- Avoid wire bonding
- Achieve better RF matching
- Design to working product in 2 months.
- 12 bare die components integration in 13.2X13.2X1.5mm package



J.A.M.E.S. Coin

Key features

- Educational design
- Easy circuit based on small smd components
- Avoid soldering
- Embedded components
- Explore new ways of printing processes
- Totally open source and shared through the community



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